CLAIMS

1. A semiconductor element having a semiconductor layer comprising a source area, a drain area, and a gate area, agate insulating film, a source electrode, a drain electrode, and a gate electrode formed on said gate insulating film, formed on a substrate; wherein:

said gate electrode comprises:

two upper and lower layer comprising a silicide thin film and a metal thin film, one of the thin films is a gate electrode serving also as an LDD forming mask, formed by slightly protruding on at least one of the source electrode side and the drain electrode side of the other thin film; and

said semiconductor layer having:

an LDD area formed in an area corresponding to the gate electrode position determinable from the positions of said silicide thin film and said metal thin film and the injecting direction of impurity ions because impurity ions are injected with said gate electrode serving also as an LDD forming said LDD forming mask as the injecting mask.

2. A semiconductor element having a semiconductor layer comprising a source area, a drain area, and a gate area, a gate insulating film, a source electrode, a drain

electrode, and a gate electrode formed on said gate insulating film, formed on a substrate; wherein:

said gate electrode comprises:

upper and lower silicide thin films, one of said thin films being a gate

electrode serving also as an LDD forming mask formed in slight protrusion on at least the source

electrode side and the drain electrode side of the other thin film;

said semiconductor layer having:

an LDD area formed in an area corresponding to the gate electrode position determinable from the positions of said silicide thin film and said metal thin film and the injection direction of impurity ions because impurity ions are injected with said gate electrode serving also as an LDD forming said LDD forming mask as the injecting mask.

3. A semiconductor element having a semiconductor layer comprising a source area, a drain area, and a gate area, a gate insulating film, a source electrode, a drain

electrode, and a gate electrode formed on said gate insulating film, formed on a substrate; wherein:

said gate electrode is:

a multi-stage gate electrode serving also as a mask for forming an LDD, comprising a plurality of layers having at least a silicide thin film, a metal thin film and a silicon thin film, which is, as a mask used when injecting impurities, the thickest at the center portion, the thinnest at both ends, and has a middle portion having a medium thickness, or which is thicker from the both ends toward the center portion; and

said semiconductor layer having:

a multi-stage LDD area formed at a position dependent on said mask thickness and the inducting direction of impurity ions, since impurity ions

are injected from above with said gate electrode serving also as an LDD forming mask.

4. A semiconductor element having a semiconductor layer comprising a source area, a drain area, and a gate area, a gate insulating film, a source electrode, a drain
electrode, and a gate electrode formed on said gate insulating film, formed on a substrate; wherein:

said gate electrode being:

an intermediate aluminum gate electrode serving also as an LDD mask, comprising a layer comprising a high-melting-point metal thin film;

a layer comprising a silicide thin film; and

a layer comprising an aluminum thin film surrounded by said high-melting-point metal thin film and said silicide thin film; the mask thickness being the largest at the center portion and smaller toward the both ends thereof; and

said semiconductor layer being:

an LDD semiconductor element being:

an LDD semiconductor element having a single-stage or multi-stage LDD area formed at a position dependent upon the mask thickness and the injecting direction of
impurities since impurity ions are injected from above, using said intermediate aluminum layer gate electrode serving also as an LDD mask as an injecting mask.

5. A semiconductor element according to claim 1, 2, 3 or 4, wherein:

said silicide thin film is a silicide thin film comprising a specific material selected from the group consisting of titanium silicide, cobalt silicide, nickel silicide, zirconium silicide, molybdenum silicide, palladium silicide, and platinum silicide.

6. A semiconductor element according to claim 5, wherein:

said at least one metal thin film or a high-melting-point metal thin film is a metal thin film in which the component metal element is the same as the metal element composing said silicide.

7. A semiconductor element according to claim 1, 2, 3 or 4, wherein:

said semiconductor element has silicide thin films of the same material as that of the silicide thin film of said gate electrode at a contact portion of said source electrode and said source area, and at a contact portion of said drain electrode and said drain area.

8. A semiconductor element according to claim 5, wherein:

said semiconductor element has silicide thin films of the same material as that of the silicide thin film of said gate electrode at a contact portion of said source electrode and said source area, and at a contact portion of said drain electrode and said drain area.

9. A semiconductor element according to claim 6, wherein:

said semiconductor element has silicide thin films of the same

material as that of the silicide thin film of said gate electrode at a contact portion of said source electrode and said source area, and at a contact portion of said drain electrode and said drain area.

10. A manufacturing method of a semiconductor element, comprising the steps of:

a basic forming step for forming a semiconductor layer at a prescribed position on a substrate and forming a gate insulating film on the thus formed semiconductor layer;

a gate electrode forming step for forming a gate electrode serving also as a mask for use upon injecting impurities, having a structure in which said gate electrode has at least one silicide thin film on the thus formed gate insulating film, and at least one of said thin films protrudes in a direction of at least one of the source electrode and the drain electrode of the other thin films, and when injecting impurities, the mask has the largest thickness at the center portion and gradually smaller thickness in the protruding direction in a direction of at least one of the source electrode and the drain electrode; and

an injecting step for forming a semiconductor layer having an LDD structure comprising, when injecting impurity ions into said semiconductor layer, using the thus formed gate electrode as an injecting mask, a source area and a drain area having a large amount of injection of impurity ions because of the non-existence of a mask, an LDD area having a small amount of impurity ion injection because only the protruding portion serves as a mask, and a channel area having no injection of impurity ions because all

the thin films serve as masks.

11. A manufacturing method of a semiconductor element, comprising the steps of:

a basic forming step for forming semiconductor layer at a prescribed position on a substrate, and forming a gate insulating film on the thus formed semiconductor layer;

a lower thin film forming step for forming a silicon thin film or a metal thin film serving as a lower layer of a multi-layer gate electrode on the thus formed gate insulating film;

a gate electrode forming step for preliminarily forming a gate electrode having upper and lower layers of different materials by forming a metal thin film or a silicon thin film as an upper layer so that not only the thus formed lower thin film is completely covered, but also there is a protrusion in the direction of a channel area;

a silicide layer forming step for exposing the substrate having said gate electrode formed thereon to a prescribed temperature, and causing a reaction between said silicon thin film and said metal thin film, thereby forming a silicide layer in the interface between these two layers; and

an injecting step for forming a semiconductor layer having a structure which comprises, when carrying out injection of impurity ions, by using said gate electrode
preliminarily formed in said gate electrode forming step or said gate electrode including said silicide layer formed in said silicide layer forming step as a mask, a source area and a drain area having a large amount of

injected impurity ions because of the complete absence of the mask, an LDD area having a small amount of injected impurity ions because only the protruding por tion serves as the mask, and a channel area for which no impurity ion injection is performed because of the overlapping of said upper and lower layers.

12. A manufacturing method of a semiconductor element according to claim 10 or 11, comprising the step of:

a gate insulating film partial removing step for once removing said gate insulating film except for a portion positioned at a lower portion of said gate electrode prior to said injecting step; and

a gate insulating film re-forming step for re-forming a gate insulating film on the portion where the gate insulating film has once been removed, after the completion of said injecting step.

13. A manufacturing method of a thin film semiconductor element having a top gate type LDD structure in which patterns are arranged on a substrate, comprising the step of:

a lower gate electrode forming step for forming a lower gate electrode having a prescribed shape on a gate insulating thin film formed on a patterned semiconductor layer on the substrate;

an upper gate electrode forming step for forming an upper gate electrode in close contact with the lower electrode gate so that the gate electrode has a shape having a side poorer in masking ability upon injecting impurities as compared with the center portion at least at an end on the

source electrode side and the drain electrode side by use of the lower gate electrode formed as above; and an impurity injecting step for injecting impurities onto said semiconductor layer by use of the gate electrode, as a mask, which would have a side poorer in masking ability as compared with the center portion at least at an end on said source electrode side and said drain electrode side in the aforementioned step.

14. A manufacturing method of a thin film semiconductor element having a top gate type LDD structure in which patterns are arranged on a substrate, comprising the step of:

a lower gate electrode forming step for forming a lower gate electrode having a prescribed shape on a gate insulating thin film formed on a patterned semiconductor layer on the substrate;

an impurity light injecting step for lightly injecting impurities onto said semiconductor layer, using the thus formed lower gate electrode as a mask;

an upper gate electrode forming step for forming an upper gate electrode having a portion protruding on at least one side of the source electrode side and the drain electrode side on, and in close contact with, said lower gate electrode after the completion of said impurity light injecting step; and

an impurity injecting step for injecting impurities onto said semiconductor layer, by using, as a mask, the gate electrode of the upper/lower two-stage structure, formed in said lower gate electrode forming step and said upper gate electrode forming step.

15. A manufacturing method of a thin-film semiconductor element having a top gate type LDD structure according to claim 13 or 14, wherein:

said upper gate electrode forming step is:

a mask forming step of LDD using plating of depositing a prescribed metal by plating with the lower gate electrode as an electrode.

16. A manufacturing method of a thin-film semiconductor element having a top gate type LDD structure according to claim 15, wherein:

said mask forming step of LDD using plating is a mask forming step for LDD using a prescribed plating carried out by electrolytic plating or non-electrolytic plating.

17. A manufacturing method of a thin-film semiconductor element having a top gate type LDD structure according to claim 13, wherein:

said upper gate electrode forming step has:

an etching sub-step for simultaneously etching the upper gate electrode forming film and the lower gate electrode forming film formed in close contact with each other into the shape of the lower gate electrode; and

an anode oxidizing sub-step for anode-oxidizing the etched upper gate electrode forming film.

18. A manufacturing method of a thin-film semiconductor element having a top gate type LDD structure according to claim 13 or 14, wherein:

said upper gate electrode forming step comprises:

a mask forming step for LDD using reaction causing a reaction by

exposing the lower gate electrode to a prescribed material and forming a side comprising a lower-density compound generated by the reaction on at least one of the source electrode wide and the drain electrode side.

19. A manufacturing method of a thin-film semiconductor element having a top gate type LDD structure in which patterns are arranged on a substrate, comprising the steps of:

a lower gate electrode forming step for forming a lower gate electrode having a prescribed shape on the gate insulating film formed on the semiconductor layer patterned on the substrate;

an upper gate electrode forming step for forming an upper gate electrode so that at least one of the ends of the lower gate electrode on the source electrode side and the
drain electrode side protrudes, by using at least photolithography and etching, on the thus formed lower gate electrode; and

an impurity injecting step for injecting impurities onto said semiconductor layer, using, as a mask, the gate electrode having a side poorer in masking ability as compared with the center portion on at least one of said source electrode side and the drain electrode side through the two aforementioned steps.

20. A manufacturing method of a thin film semiconductor element having a top gate type LDD structure in which patterns are arranged on a substrate, comprising:

a lower gate electrode forming step for forming a lower gate electrode

of a prescribed shape on a gate insulating film formed on a semiconductor layer patterned on a substrate;

an impurity light injecting step for lightly injecting impurities onto said semiconductor layer by use of the thus formed lower gate electrode as a mask;

an upper gate electrode forming step for forming an upper gate electrode, in close contact, so that at least one of the ends of the lower gate electrode on the source
electrode side and the drain electrode side protrudes, by using at least any of photolithography and etching, on said lower gate electrode, after the completion of said impurity light injecting step; and

an impurity injecting step for injecting impurities onto said semiconductor layer by using the gate electrode having the upper and lower two-stage structure as a mask
formed in said lower gate electrode forming step and said upper gate electrode forming step.

21. A manufacturing method of a thin film semiconductor element having a top gate type LDD structure according to claim 13, 14, 19 or 20, comprising:

a gate insulating film removing step for once removing the gate insulating film under the gate electrode of the two-stage structure used as a mask prior to said impurity injecting step after the completion of said upper gate electrode forming step; and

a gate insulating film re-forming step for forming again a gate

insulating film on the semiconductor layer at the portion where said gate insulating film has been removed after said impurity injecting step.

22. A manufacturing method of a thin film semiconductor element having a top gate type LDD structure according to claim 15, comprising:

a gate insulating film removing step for once removing the gate insulating film under the gate electrode of the two-stage structure used as a mask prior to said impurity injecting step after the completion of said upper gate electrode forming step; and

a gate insulating film re-forming step for forming again a gate insulating film on the semiconductor layer at the portion where said gate insulating film has been removed after said impurity injecting step.

23. A manufacturing method of a thin film semiconductor element of a top gate type LDD structure according to claim 21, comprising:

a hydrogen adsorptive metal film forming step for forming a hydrogen adsorptive metal film having a prescribed thickness on the semiconductor layer after said gate insulating film removing step;

a hydrogen adsorptive metal film removing step for removing the hydrogen adsorptive metal film formed on said semiconductor layer except for the source electrode portion and the contact electrode portion, prior to said gate insulating film re-forming step after said impurity injecting step; and

a hydrogen adsorptive metal film using contact hole forming step for using said remaining hydrogen adsorptive metal film when forming the

contact hole in the both
electrode forming sections on said re-formed gate insulating film for forming a source electrode and a drain electrode.

24. A manufacturing method of a thin film semiconductor element having a top gate type LDD structure according to claim 13, 14, 19 or 20, comprising:

an electrode unnecessary portion removing step for removing the protruding portion of a side of any of the upper gate electrode or the lower gate electrode from the
other electrode on the source electrode side and the drain electrode side by said mask forming step for the LDD portion, or said lower gate electrode forming step and the upper electrode forming step, after the completion of said impurity injecting step.

25. A manufacturing method of a thin film semiconductor element having a top gate type LDD structure according to claim 15, comprising:

an electrode unnecessary portion removing step for removing the protruding portion of a side of any of the upper gate electrode or the lower gate electrode from the
other electrode on the source electrode side and the drain electrode side by said mask forming step for the LDD portion, or said lower gate electrode forming step and the upper electrode forming step, after the completion of said impurity injecting step.

26. A manufacturing method of a thin film semiconductor element having a top gate type LDD structure according to claim 21, comprising:

an electrode unnecessary portion removing step for removing the protruding portion of a side of any of the upper gate electrode or the lower gate electrode from the
other electrode on the source electrode side and the drain electrode side by said mask forming step for the LDD portion, or said lower gate electrode forming step and the upper electrode forming step, after the completion of said impurity injecting step.

27. A manufacturing method of a thin film semiconductor element having a top gate type LDD structure according to claim 23, comprising:

an electrode unnecessary portion removing step for removing the protruding portion of a side of any of the upper gate electrode or the lower gate electrode from the
other electrode on the source electrode side and the drain electrode side by said mask forming step for the LDD portion, or said lower gate electrode forming step and the upper electrode forming step, after the completion of said impurity injecting step.

28. A manufacturing method of a thin film semiconductor having a bottom gate type LDD structure, pattern-arranged on a substrate, comprising:

a gate electrode forming step for forming a prescribed gate electrode patterned on the substrate;

an upper element composing layer forming step for sequentially forming a gate insulating layer, a patterned semiconductor layer and/or an underlayer insulating layer on the thus formed gate electrode;

a main mask forming step for forming a main mask directly on said gate electrode of the uppermost layer formed in said upper element composing layer forming step;

an upper mask forming step for forming a side poorer in masking ability upon injecting impurities as compared with the center portion on at least one end of the source electrode side and the drain electrode side, by use of the thus formed main mask; and

an impurity injecting step for injecting impurities onto said semiconductor layer from above, by using the thus formed main mask and the upper mask as masks.

29. A manufacturing method of a thin film semiconductor having a bottom gate type LDD structure, pattern-arranged on a substrate, comprising:

a gate electrode forming step for forming a prescribed gate electrode patterned on the substrate;

an upper element composing layer forming step for sequentially forming a gate insulating layer, a patterned semiconductor layer and/or an underlayer insulating layer on the thus formed gate electrode;

a main mask forming step for forming a main mask directly on said gate electrode of the uppermost layer formed in said upper element composing layer forming step;

an impurity light injecting step for lightly injecting impurities onto said semiconductor layer by using the thus formed main mask as a mask;

an upper mask forming step for forming, in close contact with said main mask, an upper mask having a portion protruding on at least one end of the source electrode side and the drain electrode side, by using the thus formed main mask after the completion of said impurity light injecting step; and

an impurity injecting step for injecting impurities onto said semiconductor layer, by using said main mask and the upper mask as masks.

30. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 28 or 29, wherein:

said main mask forming step comprises:

a photosensitive resin layer forming sub-step for forming a photosensitive resin layer further on the uppermost layer formed in said upper element comprising layer forming step;

a gate electrode corresponding exposing sub-step for irradiating an electromagnetic wave of a short wavelength from the side of the substrate having said photosensitive resin layer formed thereon with said gate electrode as a mask to prevent the portion of the photosensitive remain corresponding to said gate electrode from being exposed; and

a photosensitive resin non-exposure use main mask forming sub-step for forming said main mask by using the portion not exposed of said

photosensitive resin in said gate electrode corresponding exposing sub-step, irrespective of whether the portion not exposed of said photosensitive resin is used as it is or another material is used for forming.

31. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 28 or 29, wherein:

said main mask forming step uses a metal as a main mask; and

said upper mask forming step is a plating-using upper mask forming step for depositing a prescribed metal by plating, using the main mask as one of the electrodes.

32. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 30, wherein:

said main mask forming step uses a metal as a main mask; and

said upper mask forming step is a plating-using upper mask forming step for depositing a prescribed metal by plating, using the main mask as one of the electrodes.

33. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 28 or 29, wherein:

said upper mask forming step is:

a reaction-using upper mask forming step for forming a side comprising a low-density compound, produced by exposing the main mask to

a prescribed article to cause a reaction, on at least one of the source electrode side and the drain electrode side thereof.

34. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 30, wherein:

said upper mask forming step is:

a reaction-using upper mask forming step for forming a side comprising a low-density compound, produced by exposing the main mask to a prescribed article to cause a reaction, on at least one of the source electrode side and the drain electrode side thereof.

35. A manufacturing method of a thin film semiconductor element, having a bottom gate type LDD structure, pattern-arranged on a substrate, comprising:

a gate electrode forming step for forming a prescribed gate electrode patterned on the substrate;

an upper element composing layer forming step for sequentially forming a gate insulating film, a patterned semiconductor layer and/or an underlayer insulating layer
on the thus formed gate electrode;

a main mask forming step for forming a main mask directly on said gate electrode of an uppermost layer formed in said upper element composing layer forming step;

an upper mask forming step for forming an upper mask having a side poorer in masking ability upon injecting impurities as compared with the

center portion at least at an end of the source electrode side and the drain electrode side by using the thus formed main mask by a method using at least photolithography and etching; and

an impurity injecting step for injecting impurities onto said semiconductor layer from above, with the thus formed main mask and the upper mask as masks.

36. A manufacturing method of a thin film semiconductor element, having a bottom gate type LDD structure, pattern-arranged on a substrate, comprising:

a gate electrode forming step for forming a prescribed gate electrode patterned on the substrate;

an upper element composing layer forming step for sequentially forming a gate insulating film, a patterned semiconductor layer and/or an underlayer insulating layer
on the thus formed gate electrode;

a main mask forming step for forming a main mask directly on said gate electrode of an uppermost layer formed in said upper element composing layer forming step;

an impurity light injecting step for lightly injecting impurities onto said semiconductor layer, with the thus formed main mask as a mask;

an upper mask forming step for forming an upper mask having a portion protruding on at least an end of the main mask on the source electrode side and the drain electrode side after the completion of said impurity light injecting step; and

an impurity injecting step for injecting impurities onto said semiconductor layer, by using said main mask and said upper mask as masks.

37. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 35 or 36, wherein:

said main mask forming step comprises:

a photosensitive resin layer forming sub-step for forming a photosensitive resin layer further on the uppermost layer formed in said upper element composing layer forming step;

a gate electrode corresponding exposing sub-step for irradiating an electromagnetic wave of a wavelength shorter than that of the visible beam from the side of the substrate having said photosensitive resin layer formed thereon with said gate electrode as a mask to prevent the portion of the photosensitive resin corresponding to said gate electrode from being exposed; and

a photosensitive resin non-exposure use main mask forming sub-step for forming said main mask by using the portion not exposed of said photosensitive resin in said gate electrode corresponding exposing sub-step, irrespective of whether the portion not exposed of said photosensitive resin is used as it is or another material is used for forming.

38. A manufacturing method of a thin film semiconductor element having a bottom gate LDD structure according to claim 28, 29, 30, 31, 32, 33,

34, 35 or 36, wherein:

said impurity injecting step comprises:

a bare semiconductor layer impurity injecting step for injecting impurities onto the upper surface of said semiconductor layer in the absence of an interlayer dielectric; and has:

an interlayer dielectric forming step for forming an interlayer dielectric on said semiconductor layer, after removing said main mask and said mask for LDD section, after the completion of said impurity injecting step.

39. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 30, wherein:

said impurity injecting step comprises:

a bare semiconductor layer impurity injecting step for injecting impurities onto the upper surface of said semiconductor layer in the absence of an interlayer dielectric; and has:

an interlayer dielectric forming step for forming an interlayer dielectric on said semiconductor layer, after removing said main mask and said mask for LDD section, after the completion of said impurity injecting step.

40. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 31, wherein:

said impurity injecting step comprises:

a bare semiconductor layer impurity injecting step for injecting

impurities onto the upper surface of said semiconductor layer in the absence of an interlayer dielectric; and has:

an interlayer dielectric re-forming step for forming an interlayer dielectric on said semiconductor layer, after removing said main mask and said mask for LDD section, after the completion of said impurity injecting step.

41. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 38, comprising:

a hydrogen adsorptive metal film forming step for forming a hydrogen adsorptive metal film having a prescribed thickness on the semiconductor layer, before said impurity injecting step after said upper element layer forming step;

a hydrogen adsorptive metal film removing step for removing the hydrogen adsorptive metal film formed on said semiconductor layer except for the source electrode portion and the contact electrode portion, prior to said gate insulating film re-forming step after said impurity injecting step; and

a hydrogen adsorptive metal film using contact hole forming step for using said remaining hydrogen adsorptive metal film when forming the contact hole in the both electrode forming sections of said re-formed gate insulating film for forming a source electrode and a drain electrode.

42. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 39, comprising:

a hydrogen adsorptive metal film forming step for forming a hydrogen adsorptive metal film having a prescribed thickness on the semiconductor, before said impurity injection step after the completion of said upper element layer forming step;

a hydrogen adsorptive metal film removing step for removing the hydrogen adsorptive metal film on said semiconductor except for the source electrode portion and the contact electrode portion, prior to said interlayer dielectric re-forming step after said impurity injecting step; and

a hydrogen adsorptive metal using contact hole forming step for using said remaining hydrogen adsorptive metal film as an etching stopper, when forming a contact hole in the both electrode forming portion on said re-formed interlayer dielectric for forming a source electrode and a drain electrode.

43. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 40, comprising:

a hydrogen adsorptive metal film forming step for forming a hydrogen adsorptive metal film having a prescribed thickness on the semiconductor, before said impurity injecting step after the completion of said upper element layer forming step;

a hydrogen adsorptive metal film removing step for removing the hydrogen adsorptive metal film formed on said semiconductor except for the source electrode portion and the contact electrode portion, prior to said interlayer dielectric re-forming step after said impurity injecting step and

a hydrogen adsorptive metal using contact hole forming step for using

said remaining hydrogen adsorptive metal film as an etching stopper, when forming a contact hole in the both electrode forming portion on said re-formed interlayer dielectric for forming a source electrode and a drain electrode.

44. A semiconductor element having a top gate type LDD structure pattern-arranged on a substrate, comprising:

an upper gate electrode;

a lower gate electrode, at least a side thereof on the source electrode side and the drain electrode side protruding from said upper gate electrode, and formed in close contact with said upper gate electrode; and

a semiconductor section having a channel area directly below said upper gate electrode and said lower gate electrode, an LDD area directly below a protruding portion of said lower electrode, and a source area and a drain area not covered with said upper gate electrode and said lower electrode.

45. A semiconductor element having a top gate type LDD structure pattern-arranged on a substrate, comprising:

a lower gate electrode;

an upper gate electrode, at least a side thereof on the source electrode side and the drain electrode side protruding from said lower gate electrode, and formed in close contact with said lower gate electrode; and

a semiconductor section having a channel area directly below said upper gate electrode and said lower gate electrode, an LDD area directly

below a protruding portion of said lower electrode, and a source area and a drain area not covered with said upper gate electrode and said lower electrode.

46. A semiconductor element having a top gate type LDD structure according to claim 45, wherein:

said upper gate electrode is a plating type upper gate electrode formed by plating a metal onto the exterior surface of said lower gate electrode.

47. A semiconductor element having a top gate type LDD structure according to claim 44, 45 or 46, wherein:

said source electrode and said drain electrode have:

a silicide layer at a contact portion with the semiconductor layer; and

a silicide forming metal layer on said silicide layer.

48. A semiconductor element having a top gate type LDD structure according to claim 44, 45, or 46, wherein:

said gate insulating layer is formed:

directly below said upper and lower gate electrodes and/or in the proximity thereof and the other portion at different points in time.

49. A semiconductor element having a top gate type LDD structure according to claim 48, wherein:

said gate insulating layer is formed:

directly below said upper and lower gate electrodes and/or in the proximity thereof and the other portion at different points in time.

50. A semiconductor element having a top gate type LDD structure according to claim 44, 45 or 46, wherein:

one of said upper gate electrode and said lower gate electrode comprises:

a low-resistance electrode having an electric specific resistance of up to 5 Ω·cm as a result of use of a low- resistance metal material such as Cu, Al, Ag or Au; and is:

a high-masking electrode having a high masking ability of hydrogen ions injected during injection of impurities because of the use of a high-density metal material having a density of at least 8 such as W, Mo, Co, Ta, Au, Nb or Ag or a hydrogen adsorptive metal such as Zr, Ti or a Ti-based metal.

51. A semiconductor element having a top gate type LDD structure according to claim 47, wherein:

one of said upper fate electrode and said lower gate electrode comprises:

a low-resistance electrode having an electric specific resistance of up to 5 Ω·cm as a result of use of a low-resistance metal material such as Cu, Al, Ag or Au; and is:

a high-masking electrode having a high masking ability of hydrogen ions injected during injection of impurities because of the use of a

high-density metal material having a density of at least 8 such as W, Mo, Co, Ta, Au, Nb or Ag or a hydrogen adsorptive metal such as Zr, Ti or a Ti-based metal.

52. A semiconductor element having a top gate type LDD structure according to claim 48, wherein:

one of said upper gate electrode and said lower gate electrode comprises:

a low-resistance electrode having an electric specific resistance of up to 5 Ω·cm as a result of use of a low- resistance metal material such as Cu, Al, Ag or Au; and is:

a high-masking electrode having a high masking ability of hydrogen ions injected during injection of impurities because of the use of a high-density metal material having a density of at least 8 such as W, Mo, Co, Ta, Au, Nb or Ag or a hydrogen adsorptive metal such as Zr, Ti or a Ti-based metal.

53. A semiconductor element having a top gate type LDD structure according to claim 49, wherein:

one of said upper gate electrode and said lower gate electrode comprises:

a low-resistance electrode having an electric specific resistance of up to 5 Ω·cm as a result of use of a low- resistance metal material such as Cu, Al, Ag or Au; and is:

a high-masking electrode having a high masking ability of hydrogen ions injected during injection of impurities because of the use of a

high-density metal material having a density of at least 8 such as W, Mo, Co, Ta, Au, Nb or Ag or a hydrogen adsorptive metal such as Zr, Ti or a Ti-based metal.

54. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 44, 45 or 46, wherein:

said substrate comprises:

a TFT array substrate of a liquid crystal display unit; and one of said lower gate electrode and said upper gate electrode comprises:

a transparent conductive film because it is formed through the same process as that of the transparent conductive film of a pixel section.

55. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 47, wherein:

said substrate comprises:

a TFT array substrate of a liquid crystal display unit; and one of said lower gate electrode and said upper gate electrode comprises:

a transparent conductive film because it is formed through the same process as that of the transparent conductive film of a pixel section.

56. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 48, wherein:

said substrate comprises:

a TFT array substrate of a liquid crystal display unit; and one of said

lower gate electrode and said upper gate electrode comprises:

a transparent conductive film because it is formed through the same process as that of the transparent conductive film of a pixel section.

57. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 49, wherein:

said substrate comprises:

a TFT array substrate of a liquid crystal display unit; and one of said lower gate electrode and said upper gate electrode comprises:

a transparent conductive film because it is formed through the same process as that of the transparent conductive film of a pixel section.

58. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 44, 45, or 46, wherein:

said substrate comprises:

a TFT substrate of a reflection type liquid crystal display unit; and

one of said lower gate electrode and said upper gate electrode comprises:

a satisfactorily reflective metal film because it is formed through the same process as that of a reflecting film of a pixel section.

59. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 47, wherein:

said substrate comprises:

a TFT array substrate of a reflection type liquid crystal display unit; and

one of said lower gate electrode and said upper gate electrode comprises:

a satisfactorily reflective metal film because it is formed through the same process as that of a reflecting film of a pixel section.

60. A manufacturing method of a thin film semiconductor element having a bottom gate type LDD structure according to claim 50, wherein:

said substrate comprises:

a TFT array substrate of a reflection type liquid crystal display unit; and

one of said lower gate electrode and said upper gate electrode comprises:

a satisfactorily reflective metal film because it is formed through the same process as that of a reflecting film of a pixel section.

61. A top gate type semiconductor element having an upper gate electrode and a lower gate electrode, pattern-arranged on a substrate, and formed in close contact with each other one on top of the other on a gate insulating film, wherein:

one of said upper gate electrode and said lower gate electrode is:

a low-resistance electrode having an electric specific resistance of up to 5 $\Omega \cdot$cm because of the use of a low- resistance metal material such as Cu, Al, Ag and Au; and

said the other lower gate electrode or said gate electrode is a high-masking electrode having a high masking ability of hydrogen ions injected during injection of impurities because of the use of a hydrogen adsorptive metal such as W, Mo, Co, Ta, Au, Nb or Ag.

62. A top gate type semiconductor element according to claim 61, wherein:

said source electrode and said drain electrode has:

a silicide layer at a contact portion with said semiconductor layer; and a silicide forming metal layer on said silicide layer.

63. A top gate type semiconductor element according to claim 61 or 62, wherein:

said gate insulating layer is formed directly below said upper and lower gate electrodes, or in addition, in the proximity thereof and other portions at different points in time.

64. A top gate type semiconductor element pattern-arranged on a substrate, having gate electrodes comprising an upper gate electrode and a lower gate electrode formed one on top of the other in close contact with each other on a gate insulating film, wherein:

one of said upper gate electrode and said lower gate electrode is a low-resistance electrode having an electric resistance of up to 5 $\Omega \cdot$cm because of use of a low-resistance metal material such as Cu, Al, Ag or Au; and

said the other gate electrode or upper gate electrode is a high-masking electrode having a high masking ability of hydrogen ions injected during injection of impurities because of use of a high-density metal material such as W, Mo, Co, Ta, Au, Nb or Ag, or a hydrogen adsorptive metal such as Zr, Ti or a Ti-based metal.

65. A semiconductor element having a top gate type LDD structure according to claim 64, wherein:

said source electrode and said drain electrode comprises:

a silicide layer at a contact portion with the semiconductor layer; and

a silicide forming metal layer on said silicide layer.

66. A semiconductor element having a top gate type LDD structure according to claim 64 or 65, wherein:

said gate insulating layer is formed:

directly below said upper and lower gate electrodes, or in addition, in the proximity thereof and other portions at different points in time.

67. A substrate wherein:

said substrate is provided with an LDD type TFT in response to properties required, because the LDD type TFT is required to have different properties, depending upon a position on said substrate, as in a substrate having a pixel section and a driving circuit section surrounding the same integrally formed therewith, comprises:

a two-stage structure gate electrode comprising an area on the

substrate comprises a lower gate electrode, in which an upper gate electrode, and at least one of the source electrode side and the drain electrode side protrudes from said upper gate electrode, formed in close contact with said upper gate electrode, or on the contrary, in which a lower gate electrode, and at least one of the source electrode side and the drain electrode side protrudes from said lower gate electrode, formed in close contact with said lower gate electrode;

a semiconductor portion having a channel area directly below said upper gate electrode and said lower electrode, an LDD area directly below the protruding portion of said upper electrode or said lower electrode, and a source area and a drain area not covered with said upper gate electrode and said lower electrode; and

the other areas or some of the other area on the substrate comprise:

a two-stage columnar-shaped gate electrode comprising an upper gate electrode and a lower gate electrode formed in close contact with said upper gate electrode, and none of the upper and lower gate electrodes have a protruding portion, or a gate electrode serving also as a complete mask upon injecting impurities comprising a single gate electrode; and has:

a semiconductor section having a channel area directly below said gate electrode serving also as a complete mask upon injecting impurities, an LDD area on at least one of the source electrode side and the drain electrode side of said channel area, and source area and drain area at both ends of these areas.

68. A substrate according to claim 67, wherein:

said substrate is a TFT array substrate for a liquid crystal display unit;

in an LDD type TFT formed in said pixel section,

one of said upper gate electrode and said lower gate electrode is a low-resistance electrode having an electric specific resistance of up to 5 Ω · cm because of use of a low-resistance metal material such as Cu, Al, Ag or Au;

said other lower gate electrode or said gate electrode is a high-masking electrode having a high masking ability of hydrogen ions injected during injection of impurities, because of use of a high-density metal material having a density of at least 8 such as W, Mo, Co, Ta, Au, Nb or Ag, or a metal material having a high coupling ability with hydrogen such as Zr, Ti or Ti-based metal.

69. A bottom gate type semiconductor having a gate electrode comprising a multi-layer structure having silicide or a silicide layer.

70. A manufacturing method of a thin film semiconductor element having a top gate type LDD structure, which is pattern-arranged on a substrate, comprising:

a gate electrode forming step for forming a gate electrode having a prescribed shape on a gate insulating film formed on the semiconductor layer patterned on the substrate;

an etching mask forming step for forming a side serving as an etching mask upon removing said gate insulating film on at least a side of the

source electrode side and the drain electrode side, by use of the thus formed gate electrode, in close contact with the gate electrode;

a gate insulating film removing step for once removing the gate insulating film except for the portion directly below, by using the thus formed gate electrode and a side

etching mask as etching masks;

an injecting step for injecting impurities by using the said gate electrode, the gate insulating film present thereunder, or in addition, the side etching mask of the gate electrode as masks; and

a gate insulating film re-forming step for forming again the gate insulating film at the removed portion.

71. A manufacturing method of a thin film semiconductor element having a top gate type LDD structure according to claim 70, wherein:

said etching mask forming step is an etching mask forming step using plating for depositing a prescribed metal by plating with a gate electrode as an electrode.